LISTING OF CLAIMS

The following listing of claims will replace all prior versions and listings of the claims in the application:

Claim 1 (Currently amended): A system for integrated circuit (IC) design comprising:

at least one structural multi-project wafer (SMPW) comprising a plurality of pre-manufactured and pre-validated ~~functional blocks~~dice, each die configured to be separately programmed into a customized concept validating IC; and

a streamlined IC design flow ~~incorporating~~for fabricating separate ICs from each of the concept validating ICs of the SMPW, ~~and~~ the design flow having no IP integration or floor planning requirements.

Claim 2 (Currently amended): The system of claim 1, wherein the ~~functional blocks~~dice of the SMPW comprise structural arrays.

Claim 3 (Currently amended): The system of claim 1, wherein the SMPW is pre-fabricated up to a contact layer so that a user can customize and program different ~~blocks~~ones of the dice of the SMPW to the user's requirements.

Claim 4 (original): The system of claim 1, wherein the IC design flow has a cycle time of approximately 1-3 months.

Claim 5 (Currently amended): The system of claim 1, wherein the ~~functional blocks are~~dice

each have circuits chosen from a group comprising: ~~metal-programmable PLLs; master/slave DLLs; metal-programmable I/O elements; sea-of-gates; memory; and high speed serial links~~gate arrays, mixed signal blocks, analog blocks, digital blocks, and memory blocks.

Claims 6-8 (Cancelled)

Claim 9 (Currently amended): A method for designing an integrated circuit (IC) comprising:

providing a plurality of structural multi-project wafers (SMPWs), each SMPW comprising a plurality of pre-manufactured and pre-validated ~~functional blocks~~dice, each die configured to be separately programmed into a customized concept validating IC;

if one of the plurality of SMPWs meets an IC designer's requirements, proceeding to a streamlined design flow and production for fabricating separate ICs from each of the concept validating ICs, the design flow having no IP integration or floor planning requirements;

if one of the plurality of SMPWs is usable as an intermediate step, extracting at least one of a usable SMPW component~~(s)~~ and an SoC structure for use in a normal COT flow; and

if one of the plurality of SMPWs does not meet a user's requirement and is not usable as an intermediate step, extracting ~~any~~ at least one of a usable IP and an SoC structure from the plurality of SMPWs for use in a normal COT flow.

Claim 10 (original): The method of claim 9, wherein the streamlined design flow has a cycle time of 1-3 months and wherein the normal COT design flow has a cycle time of 12-24

months.

Claim 11 (Currently amended): A method for providing integrated circuit design assistance comprising:

maintaining an inventory of structural multi-project wafers (SMPWs), each SMPW comprising a plurality of pre-manufactured and pre-validated ~~functional blocks~~dice, each die configured to be separately programmed into a customized concept validating IC; and

configuring a streamlined IC design flow for fabricating separate ICs from each of the concept validating ICs of the SMPW, the design flow having no IP integration or floor planning requirements.

Claim 12 (Currently amended): A method as claimed in claim 11, wherein the ~~functional blocks~~dice are metal programmable to a user's specific requirements.

Claim 13 (Currently amended): A method as claimed in claim 11, further comprising: determining whether one of the inventory of SMPWs can meet all of a user's IC design requirements or can serve an intermediate step in a user's IC design process~~, such as market/concept validation or IP validation~~.

Claim 14 (Currently amended): A method as claimed in claim 13, further comprising:

determining whether ~~any IP useful to~~at least one of an IP component and an SoC structure satisfies a user's requirement and is contained within the inventory of SMPWs.

Claim 15 (original): A method as claimed in claim 11, and further comprising:

reducing manufacturing costs to users by sharing the SMPWs among multiple users.

Claim 16 (original): A method as claimed in claim 11, and further comprising:

maintaining a pool of validated IP that is embodied in the inventory of SMPWs.

Claim 17 (Currently amended): A method as claimed in claim 16, and further comprising:

transferring **at least one of**an IP component **and an SoC structure**from the pool of validated IP from programmable logic for use in COT flow.

Claim 18 (original): A method as claimed in claim 11, and further comprising:

facilitating migration to a COT flow with the inventory of SMPWs.

Claim 19 (original): A method as claimed in claim 11, and further comprising:

providing multiple packaging and assembly options for SMPW users.

Claim 20 (original): A method as claimed in claim 19, wherein the packaging and assembly options are chosen from a group comprising: wire bond, flip chip, BGA, plastics and ceramics.